AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 8, line 4, as follows:

In the present embodiment, as shown in Fig. 3A, a pair of data lines DL are connected with the source[[s]] of N-channel MOS transistors Tr1 and drain of N-channel MOS transistor Tr4[[,]] ~~respectively~~. The ~~drains~~ gates of the transistors Tr1 and Tr4 are connected to a word line WL. The ~~source~~ drain of the transistor Tr1 is connected with the ~~drains~~ source of an N-channel MOS transistor Tr2 and the drain of a P-channel MOS transistor Tr3. The source of the transistor Tr4 is connected with the drain[[s]] of an N-channel MOS transistor Tr5 and the source of a P-channel MOS transistor Tr6. The drain of transistor Tr2 and the source[[s]] of the transistor[[s]] ~~Tr2 and~~ Tr5 are supplied with a ground voltage. The source[[s]] of the transistors Tr3 and the drain of transistor Tr6 are supplied with a power supply voltage Vcc.

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